2.1 What is a fault?

Any undesired / unwanted condition is known as a fault.

2.1.1 Reasons for fault occurrence?

- Lightning strokes / thunderstorms / switching surges
- Tree falling
- Kites
- Birds can cause faults
- Aircraft / vehicle
- Earthquake
- Wind / ice / rain
- Deterioration of insulation / ageing
- Monkey / reptiles / snakes

Sr. No.	Causes	% of Total
1	Lightning	12
2	Wind / mechanical consideration	20
3	Appliance failure	20
4	Switching to a fault	20
5	Misc. (Trees, birds, etc.)	28

Sr. No.	Equipment	% of Total
1	O.H. lines	50
2	Wind / mechanical consideration	20
3	Appliance failure	20
4	Switching to a fault	20
5	Misc. (Trees, birds, etc.)	28

2.1.2 Type of faults

Symmetrical Faults

- LLL
- LLLG

Unsymmetrical Faults

- LG
- LL
- LLG
- LL and 3rd Ground

Sr. No.	Faults	% of Total
1	LG	70
2	LL	15
3	LLG	10
4	LL or LG	2-3
5	LLLG	2-3
6	LLL	2-3

2.2 Introduction

- Symmetrical faults are caused in power system accidentally through insulation failure of equipment or flashover of lines initiated by lighting stroke or through accidental faulty operation.
- Disconnecting the faulty part of the system by means of circuit breakers operated by protective relaying is necessary to protect against flow of heavy short circuit current. For proper choice of circuit breakers, we should study this chapter.
- Most of the system faults are not three phase faults but faults involving one line to ground or occasionally two lines to ground. Though the symmetrical faults are rare, the fault leads to most severe fault current.
- The synchronous generator during short circuit has a characteristic time-varying behavior. In the event of a short circuit, the flux per pole undergoes dynamic change with associated transients in damper and field windings.

2.3 Transients on a transmission line

- Certain simplifying assumptions are made
  1. The line fed from a constant voltage source.
  2. Short circuit takes place when the line unloaded.
  3. Line capacitance is negligible and the line can be represented by a lumped RL series circuit
- As shown in fig. 2.1 short circuit is assumed to take place at $t=0$. The parameter α controls the instant on the voltage wave when short circuit occurs. It is known form circuit theory that current after short circuit is composed of two parts i.e.

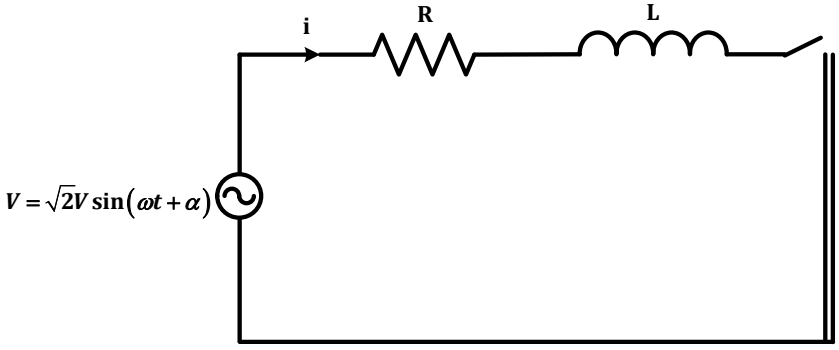

Figure 2.1 Short Circuit Model of Line

$$i = i_s + i_t$$

$i_s =$ steady state current

$$= \frac{\sqrt{2}V}{|Z|}\sin(\omega t + \alpha - \theta)$$

$$Z = \sqrt{R^2 + \omega^2 L^2} \ \angle\theta = \tan^{-1}\left(\frac{\omega L}{R}\right)$$

$i_t =$ transient current

(it is such that $i(0)=i_s(0)+i_t(0)=0$ being an inductive circuit; it decays corresponding to the time constant L/R)

- A plot of i_s, i_t, and $i=i_s+i_t$ is shown in fig. 2.2.

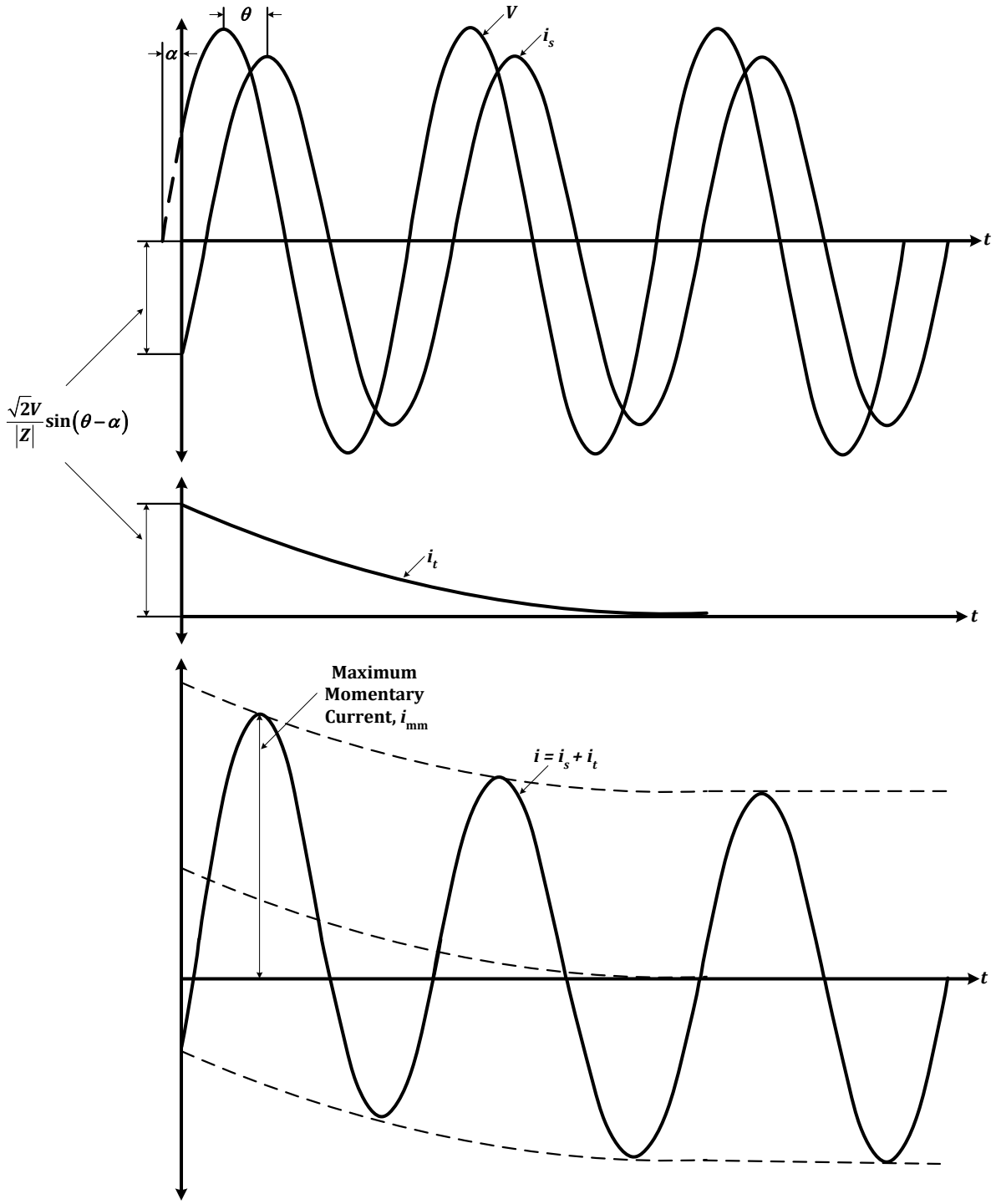

Figure 2.2 Waveform of Short Circuit Current on a Transmission Line

$$i_t = -i_s(0)e^{-(R/L)t}$$
$$= -\frac{\sqrt{2}V}{|Z|}\sin(\alpha-\theta)e^{-(R/L)t}$$
$$= \frac{\sqrt{2}V}{|Z|}\sin(\theta-\alpha)e^{-(R/L)t}$$

Thus, short circuit current is given by

$$i = \frac{\sqrt{2}V}{|Z|}\sin(\omega t+\alpha-\theta)+\frac{\sqrt{2}V}{|Z|}\sin(\theta-\alpha)e^{-(R/L)t}$$

= symmetrical SC current + DC-offset current

- In power system terminology, the sinusoidal steady state current is called the symmetrical short circuit current and the unidirectional transient component is called the DC-offset current, which causes the total short circuit to be unsymmetrical till the transient decays
- The maximum momentary current, i_{mm} corresponds to first peak. If the decay of transient in short time is neglected,

$$i_{mm} = \frac{\sqrt{2}V}{|Z|}\sin(\theta-\alpha)+\frac{\sqrt{2}V}{|Z|}$$

- Since transmission line resistance is small $\theta \cong 90°$

$$i_{mm} = \frac{\sqrt{2}V}{|Z|}\cos\alpha+\frac{\sqrt{2}V}{|Z|}$$

- This has the maximum possible value for $\alpha = 0°$, short circuit occurring when the voltage wave is going through zero.

$$i_{mm}(\text{max possible}) = \frac{2\sqrt{2}V}{|Z|}$$

= twice the maximum of symmetrical SC current (doubling effect)

- For the selection of circuit breakers, momentary short circuit current is taken corresponding to its maximum possible value (a safe choice)
- It means that when the current is interrupted, the DC offset i_t has not yet died out and so the computing the value of DC offset at the time of interruption (this would be highly complex in a small network), the symmetrical short circuit current alone is calculated. This figure is then increased by multiplying factor to take in account of the DC offset.

2.4 Short circuit of a synchronous machine (On NO Load)

- Under steady state short circuit condition, the armature reaction of a synchronous generator produces a demagnetizing flux.
- In terms of a circuit, this effect is modelled as a reactance X_a in series with the induced emf.

- This reactance when combined with the leakage reactance X_l of the machine is called synchronous reactance X_d (direct axis synchronous reactance in case of salient pole machines) as shown in fig. 2.3.

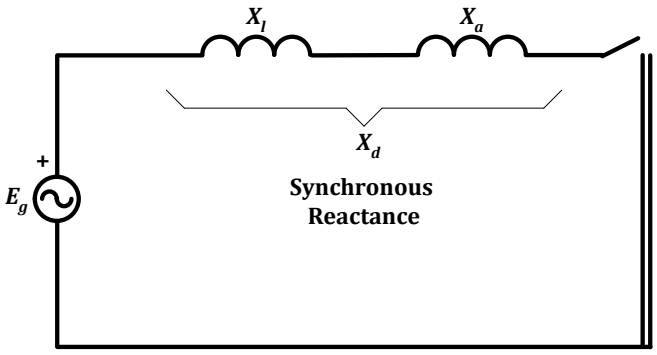

Figure 2.3 Steady State Short Circuit Model of a Synchronous Machine

- Consider now the sudden short circuit (3ϕ) of a synchronous machine initially operating under open circuit conditions.
- The circuit breaker must, of course interrupt the current much before steady conditions are reached.
- Immediately upon short circuit, the DC offset currents appear in all the three phases, each with different magnitude since the point on the voltage wave at which short circuit occurs is different for each phase.

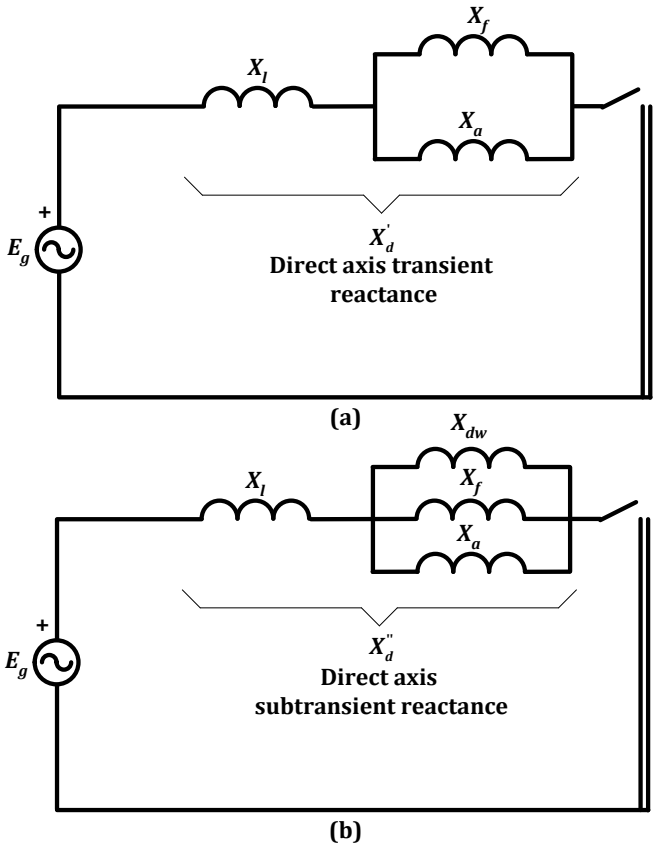

Figure 2.4 Approximate Circuit Model During (a) Subtransient Period of Short Circuit (b) Transient Period of Short Circuit

- Immediately in the event of a short circuit, the symmetrical short circuit current is limited only by leakage reactance of machine.
- Since the air gap flux cannot change instantaneously, to counter the demagnetization of the armature circuit current, current appears in field winding as well as in the damper winding in a direction to help the main flux.
- The current decays in accordance with the winding time constants. The time constant of damper winding which has low leakage inductance is much less than that of field winding with high leakage inductance.
- The machine reactance, thus changes from parallel combination of X_a, X_f and X_{dw} during the initial period (fig. 2.4 (b)) of short circuit to X_a and X_f in parallel in the middle period (fig. 2.4 (a)) of the short circuit and finally to X_a in steady state.

$$X_d'' = X_l + \frac{1}{\frac{1}{X_a} + \frac{1}{X_f} + \frac{1}{X_{dw}}}$$

$$X_d' = X_l + \frac{1}{\frac{1}{X_a} + \frac{1}{X_f}}$$

$$X_d'' < X_d' < X_d$$

$$I'' = \frac{E_g}{X_d''}$$

$$I' = \frac{E_g}{X_d'}$$

$$I = \frac{E_g}{X_d}$$

2.5 Short circuit of a loaded synchronous machine

- Fig. 2.5 shows the circuit model of a synchronous generator operating under steady conditions supplying a load current I^0 to the bus at a terminal voltage of V^0. E_g is the induced emf under loaded condition and X_d is the direct axis synchronous reactance of the machine.

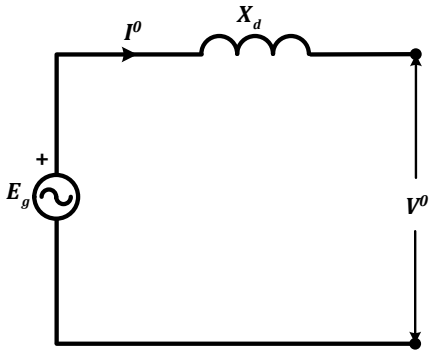

Figure 2.5 Circuit Model of a Loaded Synchronous Machine

- When short circuit occurs at the terminals of this machine, the circuit model to be used for computing short circuit current is shown in the fig. 2.6 for subtransient current and transient current.

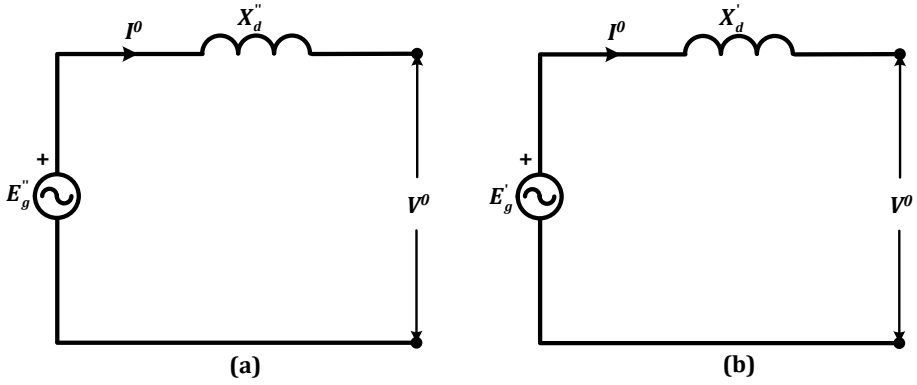

Figure 2.6 Circuit Model for Computing (a) Subtransient Current (b) Transient Current

$I^0 = I_L =$ Load current of the bus before fault

$V^0 =$ Teminal voltage

$E_g =$ Induced emf under loaded conditon

$E_g'' =$ Voltage behind subtransient reactance

$E_g' =$ Voltage behind transient reactance

$$E_g'' = V^0 + jX_d'' I^0$$
$$E_g' = V^0 + jX_d' I^0$$

- Synchronous motors have internal emfs and reactances similar to that of a generator except that the current direction is reversed. During short circuit conditions, these can be replaced by similar circuit models except that the voltage behind subtransient/transient reactance is given by

$$E_m'' = V^0 - jX_d'' I^0$$
$$E_m' = V^0 - jX_d' I^0$$

- In case of short circuit of an interconnected system, the synchronous machines (generators and motors) are replaced by their corresponding circuit models having voltage behind subtransient (transient) reactance in series with subtransient (transient) reactance. The rest of the network being passive remains unchanged.

2.6 Short circuit current by Thevenin Theorem

- An alternate method of computing short circuit current is through the application of thevenin theorem.
- Consider a synchronous generator feeding a synchronous motor over a line. Fig. 2.7 (a) shows the circuit model of the system under conditions of steady load. Fault computations are to be made for a fault at *F*, at the motor terminals.

- As a result the circuit model is replaced by the one shown in fig. 2.7 (b), wherein the synchronous machines are represented by their subtransient reactances (or transient reactances if transient currents are of interest) in series with voltages behind subtransient reactances. This change does not disturb the prefault current I^0 and prefault voltage V^0 (at *F*).

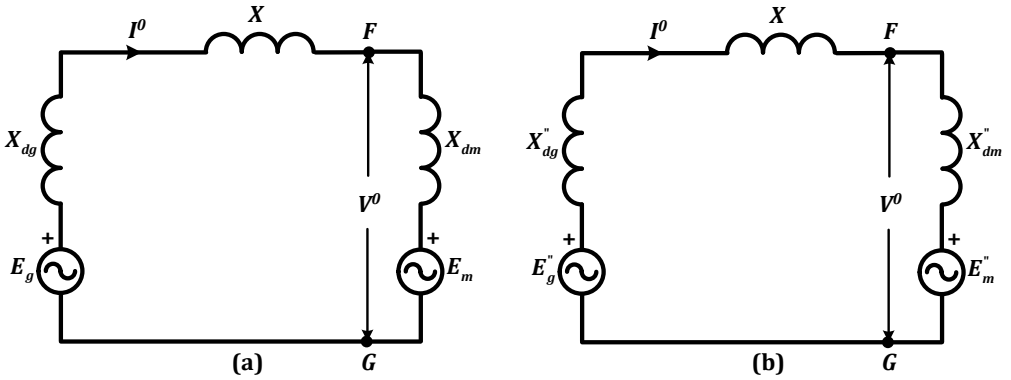

Figure 2.7 Circuit Model under (a) Steady State (b) Subtransient State

- As seen from *FG* the thevenin equivalent circuit of fig. is drawn.

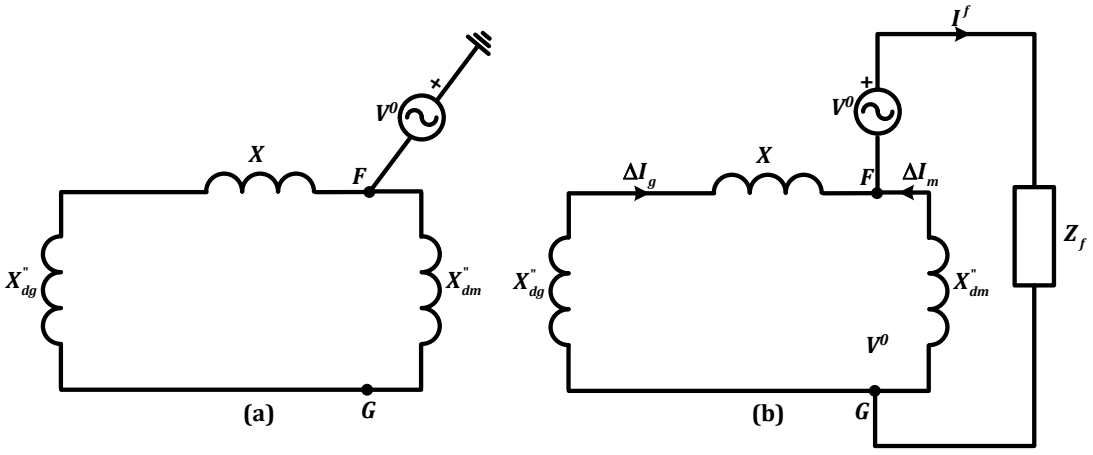

Figure 2.8 (a) Computation of SC by Thevenin Equivalent Circuit (b) Thevenin Equivalent System Feeding Fault Impedance

- Consider now a fault a *F* through an impedance Z^f. Fig. 2.8 (b) shows the thevenin equivalent of the system feeding the fault impedance.

$$X_{TH} = \left(X''_{dg} + X\right) \| X''_{dm}$$

$$X_{TH} = \frac{1}{\frac{1}{\left(X''_{dg} + X\right)} + \frac{1}{X''_{dm}}}$$

$$X_{TH} = \frac{X''_{dm}\left(X''_{dg} + X\right)}{X''_{dg} + X + X''_{dm}}$$

$$I^f = \frac{V^0}{jX_{TH} + Z^f}$$

- Current caused by fault current in generator circuit

$$\Delta I_g = \frac{X''_{dm}}{X''_{dg} + X + X''_{dm}} I^f$$

- Current caused by fault current in generator circuit

$$\Delta I_m = \frac{X''_{dg} + X}{X''_{dg} + X + X''_{dm}} I^f$$

- Postfault currents and voltages are obtained as follows by superposition:

$$I''_g = I^0 + \Delta I_g$$

$$I''_m = -I^0 + \Delta I_m \text{(in the direction of } \Delta I_m\text{)}$$

- Postfault voltage

$$V^f = V^0 + \left(-jX_{TH} I^f\right)$$

$$= V^0 + \Delta V$$

- So, the prefault current flowing out of the fault point *F* is always zero, the postfault current out of *F* is independent of load for a given prefault voltage at *F*.
- Steps for solving short circuit current by thevenin theorem approach
  1. Obtain the steady state solution using load flow. Formulate the circuit model.
  2. Replace reactance of synchronous machine by their transient or subtransient values.
  3. SC all emf sources and find the value of Z_{TH} or X_{TH}.
  4. Compute the required currents using thevenin's and superposition theorem.
- Assumptions
  1. All prefault voltage equal to 1pu.
  2. Load current neglected as it is very less as compared to SC current.

2.7 Selection of circuit breakers

- Two of the circuit breaker ratings which require the computation of SC current are: rated momentary current and rated symmetrical interrupting current.
- Symmetrical SC current is obtained by using subtransient reactances for synchronous machines. Momentary current (rms) is then calculated by multiplying the symmetrical current by a factor of 1.6 to account the presence of DC-offset current.
- The DC-offset value to be added to obtain the current to be interrupted is accounted for by multiplying the symmetrical SC current by a factor as tabulated below:

Table 2.1 Circuit Breaker Multiplying Factor

Sr. No.	Circuit breaker speed	Multiplying factor
1.	8 cycles or slower	1.0
2.	5 cycles	1.1
3.	3 cycles	1.2
4.	2 cycles	1.4

- The current that a circuit breaker can interrupt is inversely proportional to the operating voltage over a certain range, i.e.

Amperes at operating voltage = amperes at rated voltage x $\dfrac{\text{rated voltage}}{\text{operating voltage}}$

- Of course, operating voltage cannot exceed the maximum design value. Also, no matter how low the voltage is, the rated interrupting current cannot exceed the rated maximum interrupting current.
- It is therefore logical as well as convenient to express the circuit breaker rating in terms of SC MVA that can be interrupted, defined as

  Rated interrupting MVA (three phase) capacity = $\sqrt{3}x|V_{line}|x|I_{line}|_{\text{rated interrupting current}}$

  Where $|V_{line}|$ is in kV and $|I_{line}|$ is in kA

- Thus, instead of computing the SC current to be interrupted, we compute three-phase SC MVA to be interrupted, where

  SC MVA (three phase) = $\sqrt{3}$ x prefault line voltage in kV x SC current in kA

  SC MVA (three phase) = $|V|_{\text{prefault}}$ x $|I|_{SC}$ x $(\text{MVA})_{\text{Base}}$ (if in P.U.)

- Obviously, the rated MVA interrupting capacity of a circuit breaker is to be more that (or equal to) the SC MVA required to be interrupted.
- For the selection of a circuit breaker for a particular location, we must find the maximum possible SC MVA to be interrupted with respect to type and location of fault and generating capacity (also synchronous motor load) connected to the system. A three phase fault though rare is generally the one which gives the highest SC MVA and a circuit breaker must be capable of interrupting it.
- In a large system various possible location must be tried out to obtain the highest SC MVA, requires repeated SC computations.

2.8 Algorithm for SC studies

- Consider an n bus system shown schematically in fig. 2.9 operating at steady load. Consider r as faulted bus.

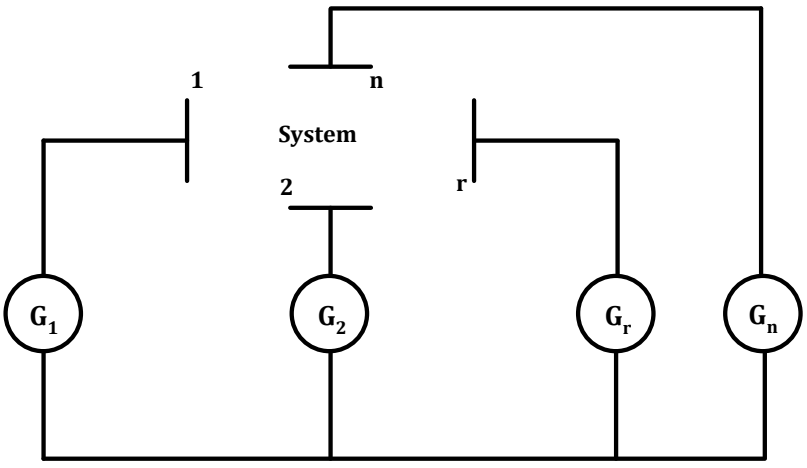

Figure 2.9 n-bus System under Steady Load

- The first step towards short circuit computation is to obtain the prefault voltages at all buses and currents in all lines through load flow studies.

- Step-1 To find out prefault voltages at all buses.

$$V_{BUS}^{0} = \begin{bmatrix} V_1^0 \\ V_2^0 \\ \vdots \\ V_n^0 \end{bmatrix}$$

- Step-2 Bus no. r is to be faulted through fault impedance Z^f

$$V_{BUS}^{f} = V_{BUS}^{0} + \Delta V \text{ (change)}$$

- Step-3 Form Thevenin's equivalent circuit. Short circuit all emf sources and replace all reactances by their respective reactances transient / sub-transient as shown in fig. 2.10

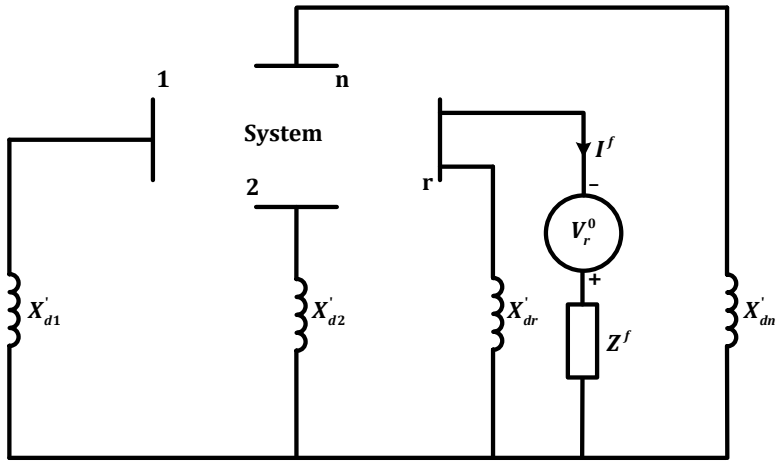

Figure 2.10 Network of System for Computing Post Fault Voltages

- Step-4 Compute the value of ΔV

$$\Delta V = Z_{BUS} J^f$$

Where,

$$Z_{BUS} = \begin{bmatrix} Z_{11} \cdots Z_{1n} \\ \vdots \quad \ddots \quad \vdots \\ Z_{n1} \cdots Z_{nn} \end{bmatrix} = \text{bus impedance matrix of the passive Thevenin network}$$

$$\mathrm{J^f} = \begin{bmatrix} 0 \\ 0 \\ -I^f \\ \vdots \\ 0 \end{bmatrix} = \text{bus current injection vector}$$

- Step-5 Find the post fault voltage for the rth bus

$$\Delta V_r = -Z_{rr} I^f$$
$$V_r^f = V_r^0 + \Delta V_r$$
$$V_r^f = V_r^0 - Z_{rr} I^f$$

$$V_r^0 = Z^f I^f + Z_{rr} I^f$$

$$I^f = \frac{V_r^0}{\left(Z^f + Z_{rr}\right)}$$

- Step-6 Find the post fault voltage for any i[th] bus

$$\Delta V_i = -Z_{ir} I^f$$

$$V_i^f = V_i^0 + \Delta V_i$$

$$V_i^f = V_i^0 - Z_{ir} I^f$$

$$V_f^0 = V_i^0 - Z_{ir} \frac{V_r^0}{\left(Z^f + Z_{rr}\right)} \quad \left(\because I^f = \frac{V_r^0}{\left(Z^f + Z_{rr}\right)} \right)$$

- Step-7 Find the post fault current in lines

$$I_{ij}^f = Y_{ij}\left(V_i^f - V_j^f\right)$$

2.9 Z_{BUS} formation by step by step method

Notation: i, j – old buses; r – reference bus; k – new bus.

i) Type-1 Modification: - Branch Z_b is added between new bus and reference bus

ii) Type-2 Modification: - Branch Z_b is added between new bus and old bus

iii) Type-3 Modification: - Branch Z_b is added between old bus to reference bus

iv) Type-4 Modification: - Branch Z_b is added between two old buses

- Type-1 Modification: - Adding a branch Z_b between new bus k and reference bus r as shown in fig 2.11.

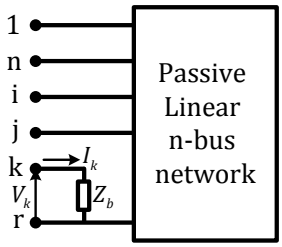

Figure 2.11 Type-1 Modification

$$V_k = Z_b I_k$$

$$Z_{ik} = Z_{ki} = 0;\ i = 1,2,...,n$$

$$Z_{kk} = Z_b$$

$$Z_{BUS}(\text{new}) = \left[\begin{array}{c|c} Z_{BUS}(\text{old}) & \begin{matrix}0\\ \vdots\\ \vdots\\ \vdots\end{matrix} \\ \hline \begin{matrix}0 & \cdots & \cdots & 0\end{matrix} & Z_b \end{array}\right]$$

- Type-2 Modification: - Adding a branch Z_b between old bus j and new bus k as shown in fig. 2.12.

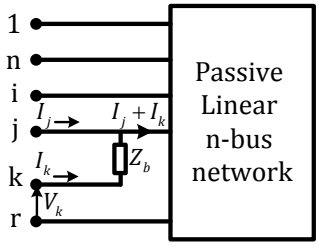

Figure 2.12 Type-2 Modification

$$V_k = Z_b I_k + V_j$$
$$= Z_b I_k + Z_{j1} I_1 + Z_{j2} I_2 + ... + Z_{jj}\left(I_j + I_k\right) + ... + Z_{jn} I_n$$

Rearranging,

$$V_k = Z_{j1} I_1 + Z_{j2} I_2 + ... + Z_{jj} I_j + ... + Z_{jn} I_n + \left(Z_{jj} + Z_b\right) I_k$$

$$Z_{BUS}(\text{new}) = \left[\begin{array}{ccc|c} & Z_{BUS}(\text{old}) & & \begin{matrix} Z_{1j} \\ Z_{2j} \\ \vdots \\ Z_{nj} \end{matrix} \\ \hline Z_{j1} & Z_{j2} \cdots & Z_{jn} & Z_{jj} + Z_b \end{array}\right]$$

- Type-3 Modification: - Adding a branch Z_b between old bus j and reference bus r as shown in fig. 2.13. This case follows by connecting bus k to the reference bus r, i.e., by setting $V_k = 0$.

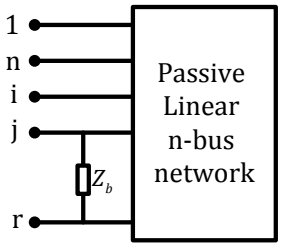

Figure 2.13 Type-3 Modification

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \\ 0 \end{bmatrix} = \left[\begin{array}{ccc|c} & Z_{BUS}(\text{old}) & & \begin{matrix} Z_{1j} \\ Z_{2j} \\ \vdots \\ Z_{nj} \end{matrix} \\ \hline Z_{j1} & Z_{j2} \cdots & Z_{jn} & Z_{jj} + Z_b \end{array}\right] \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \\ I_k \end{bmatrix}$$

Eliminate I_k in the set of equations contained in the matrix,

$$0 = Z_{j1}I_1 + Z_{j2}I_2 + ... + Z_{jn}I_n + \left(Z_{jj} + Z_b\right)I_k$$

$$I_k = -\frac{1}{Z_{jj} + Z_b}\left(Z_{j1}I_1 + Z_{j2}I_2 + ... + Z_{jn}I_n\right)$$

Now,

$$V_i = Z_{i1}I_1 + Z_{i2}I_2 + ... + Z_{in}I_n + Z_{ij}I_k$$

$$V_i = \left[Z_{i1} - \frac{1}{Z_{jj} + Z_b}\left(Z_{ij}Z_{j1}\right)\right]I_1 + \left[Z_{i2} - \frac{1}{Z_{jj} + Z_b}\left(Z_{ij}Z_{j2}\right)\right]I_2 + ... + \left[Z_{in} - \frac{1}{Z_{jj} + Z_b}\left(Z_{ij}Z_{jn}\right)\right]I_n$$

In matrix form,

$$Z_{BUS}(\text{new}) = Z_{BUS}(\text{old}) - \frac{1}{Z_{jj} + Z_b}\begin{bmatrix} Z_{1j} \\ Z_{2j} \\ \vdots \\ Z_{nj} \end{bmatrix}\begin{bmatrix} Z_{j1} & Z_{j2} & \cdots & Z_{jn} \end{bmatrix}$$

- Type-4 Modification: - Adding a branch Z_b between old bus i and old bus j in fig. 2.14.

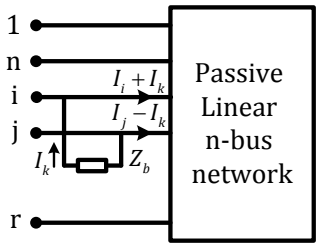

Figure 2.14 Type-4 Modification

$$V_i = Z_{i1}I_1 + Z_{i2}I_2 + ... + Z_{ii}\left(I_i + I_k\right) + Z_{ij}\left(I_j - I_k\right) + ... + Z_{in}I_n$$

Similar equations follow for other buses. The voltages of the buses i and j are, however, constrained by the equation

$$V_j = Z_b I_k + V_i$$

$$Z_{j1}I_1 + Z_{j2}I_2 + ... + Z_{ji}\left(I_i + I_k\right) + Z_{jj}\left(I_j - I_k\right) + ... + Z_{jn}I_n =$$

$$Z_b I_k + Z_{i1}I_1 + Z_{i2}I_2 + ... + Z_{ii}\left(I_i + I_k\right) + Z_{ij}\left(I_j - I_k\right) + ... + Z_{in}I_n$$

Rearranging,

$$0 = \left(Z_{i1} - Z_{j1}\right)I_1 + ... + \left(Z_{ii} - Z_{ji}\right)I_i + \left(Z_{ij} - Z_{jj}\right)I_j + ... + \left(Z_{in} - Z_{jn}\right)I_n + \left(Z_b + Z_{ii} + Z_{jj} - Z_{ij} - Z_{ji}\right)I_k$$

In matrix form,

$$\begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \\ \hline 0 \end{bmatrix} = \left[\begin{array}{ccc|c} & Z_{BUS}(\text{old}) & & \begin{matrix} (Z_{1i}-Z_{1j}) \\ (Z_{2i}-Z_{2j}) \\ \vdots \\ (Z_{ni}-Z_{nj}) \end{matrix} \\ \hline (Z_{i1}-Z_{j1}) & (Z_{i2}-Z_{j2}) & \cdots & (Z_{in}-Z_{jn}) \quad Z_b+Z_{ii}+Z_{jj}-2Z_{ij} \end{array}\right] \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \\ I_j \end{bmatrix}$$

Eliminate I_k on lines similar to what was done in type-2 modification, it follows that

$$Z_{BUS}(\text{new}) = Z_{BUS}(\text{old}) - \frac{1}{Z_{ii}+Z_{jj}+Z_b-2Z_{ij}} \begin{bmatrix} Z_{1i}-Z_{1j} \\ Z_{2i}-Z_{2j} \\ \vdots \\ Z_{ni}-Z_{nj} \end{bmatrix} \left[(Z_{i1}-Z_{j1}) \quad (Z_{i2}-Z_{j2}) \quad \cdots \quad (Z_{in}-Z_{jn}) \right]$$